IN THE SPECIFICATION

Please Amend the paragraph beginning on page 7, line 16 in accordance with the following markup copy:

Additionally, in an actual integrated circuit layout, input/output (I/O) blocks are generally large with respect to other circuits due to the drive requirement of the transmitters and power dissipation in the receivers, so it may not be possible to co-locate all of the I/O blocks associated with a given interface. In this case, it would not be desirable to route a single reference signal between I/O blocks that are far apart on an actual integrated circuit die. Common-mode noise and voltage levels will vary between distant blocks. Therefore it is more desirable to use a differential data pair associated in [[a]] common I/O blocks for detection of single-ended data signals in order to provide the best tracking and common-mode noise rejection for that group of signals.

Please Amend the paragraph beginning on page 8, line 27 in accordance with the following markup copy:

Referring now to **Figure 2**, a schematic diagram of a singlential receiver in accordance with a preferred embodiment of the invention is depicted. A differential comparator **K1** compares signals **A** and **/A** to produce an output signal that is latched by a latch **D1** to produce an output data signal **A Out**. A level shift **21** is coupled to the output of comparator **K1** to remove shift in the logic low output level of the comparator due to the presence of common mode voltage on the input signals. Latch **D1** latches the output of level shift **21** on the rising edge of **IOCLK** (**IOCLK** is a clock signal derived such that data will be stable at the outputs of comparator **K1** when **IOCLK** rises). A novel singlential comparator **K2** receives the differential pair comprising signals **A** and **/A** as well as single-ended data signal **B**. Singlential comparator **K2** detects data signal **B** such that a common-mode voltage appearing on signals **B**, **A**, and **/A** is rejected. A level shift **23** ~~is~~ couples the output of singlential comparator **K2** to a latch **D2**. Level shift **23** removes variations in the logic low voltage level on the output of singlential comparator **K2** due to the presence of common mode voltage on the input signals.

Please Amend the paragraph beginning on page 9, line 30 in accordance with the following markup copy:

Referring now to **Figure 3A**, a detailed schematic of differential comparator **K1** of **Figure** [[**1**]] **2** is depicted. N-channel transistor **N1** and N-channel transistor **N2** form a differential pair. When the voltage of data signal **A** is higher than the voltage of complementary data signal **/A**, N-channel transistor **N1** will provide the majority of the current sourced into constant-current sink **I1**, causing the voltage at **Out A** to assume a high logic level. Conversely when the voltage of data signal **A** is lower than the voltage of complementary data signal **/A**, N-channel transistor **N2** will provide the majority of the current sourced into constant-current sink **I1**, causing the voltage at **Out A** to assume a low logic level by drawing current through resistor **R1** which has a resistance value of **R**.